WIDEBAND VARIABLE GAIN AMPLIFIERS IN GAAS MMIC

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ABSTRACT

The design and performance of C, X, and K_u-band GaAs MMIC variable gain and variable power amplifier circuits using an improved segmented dual gate MESFET device with binary scaled gate width ratios is reported. The demonstrated 35 dB control range, flat octave band gain response, and less than 10 degrees incidental phase variation as a function of gain/attenuation state over a 20 dB control range, is significantly superior to conventional analog-controlled devices. First pass performance of these digitally-controlled circuits demonstrates the maturation of MMIC technology.

INTRODUCTION

Future aerospace systems, such as multifunction active phased array radar and wideband communication systems require precise amplitude control in order to achieve the improved transmit/receive sidelobe levels demanded by the modern electromagnetic environment. Digitally-controlled programmability imposes additional constraints that have evolved from adaptive pattern control requirements. The objective of this work was to develop variable gain amplifier (VGA) and variable power amplifier (VPA) circuits using dual gate MESFET's in order to provide transmit/receive architectures with precise amplitude quantization over a 30 to 40 dB control range while minimizing insertion phase variations, and thus calibration complexity, incurred by gain state switching. Wide bandwidth, enabling generic application, and compactness were additional objectives, leading to low cost, high yield fabrication.

MESFET DEVICE

Following the results of Hwang [1], the amplifier circuits developed here use segmented dual gate MESFET's (SDGFET's) to obtain precise gain control. In this approach, the second gate of the dual gate MESFET is digitally-controlled to selectively switch on/off portions of the SDGFET total gate periphery in order to achieve a desired gain state. The on/off control is achieved by switching the gate #2 bias voltage levels between saturation and pinch-off, making the device CMOS compatible, while the gate #1 voltage is held constant. When the reference maximum gain state of the SDGFET is chosen such that all segments of the device are biased on, a specific gain/attenuation level can be selected by turning off portions of the total SDGFET periphery. If the segments are scaled in a binary fashion, a linear gain/attenuation curve results with 6 dB steps between MSB states. From a pattern control viewpoint, this scale is desireable, as it provides finer weight control of center elements and the faster peripheral roll-off of typical weighting functions.

Harris Microwave Semiconductor selectively implanted 0.5 um gate length devices were utilized as the basis for the designs. These planar devices fabricated on low-pressure LEC material employ a dual level plating scheme to achieve a large cross-section low-resistance plated T-shaped gate as well as source air bridge interconnection. De-embedded small-signal S-parameters of a 200 μm periphery dual gate device were measured from 0.5 to 20 GHz with the second gate short-circuited to ground and with a voltage beyond pinch-off applied. Equivalent circuits including fixturing and gate #2 termination parasitics for both the on and the off state were then fitted to the data.

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Figure 1 depicts the monolithic dual gate circuit model used for small-signal circuit design with element values given for both states at the bias point of 4V and 20% of I_{dss}. Unlike the dual gate model used in [1], this improved model consists of two single gate FET devices in series, augmented with gate #1 to gate #2 and gate #1 to drain capacitances. Note that it is difficult to model a dual gate GaAs MESFET because of its complicated geometry and the effect of the terminal impedance at gate #2, and thus extreme care in fixturing, de-embedding, and modeling is required since this base model will be scaled up and down in periphery to obtain the SDGFET model as a function of gain/attenuation state.

CIRCUIT DESIGN

In order to obtain the small-signal models required for circuit design, on/off state models were generated for the MSB segments via binary scaling of the Figure 1 models. By paralleling the segment models, the MSB state models were generated. For the VGA designs, several factors influence the size of the segments, including power consumption, circuit size, and dynamic range requirements. Six-bits were required resulting in a 450 μm total gate periphery consisting of 200, 100, 50, and 25 μm segments. The last two-bits were obtained using a resitive divider and 50/25 μm segments, in order to avoid fringing effects which perturb scaling rules when small peripheries are required. As an amplifier, the SDGFET is operated in a cascode configuration with the second gate RF grounded via a shunt capacitor and uses resistors for isolation from the control voltage source. The relative phase shift of the VGA between states, referenced to the case where all segments of the device are turned on, can be minimized by proper selection of the gate #2 termination capacitors. These capacitors scale in proportion to the gate width of the particular segment being terminated.

The variable power amplifier (VPA) subsequently described required three-bits of control per stage and consequently, 800, 400, and 200 μm segments were selected. In order to prevent self-bias under power conditions, the gate #2 isolation resistors were reduced to values that allowed the control voltage to source/sink the milliamps of current required. In addition to operation at the power bias point of 8V and 60% of I_{dss}, a class A power amplifier design technique was required for the variable power amplifier. Large-signal circuit design utilized a modified version of the methodology described in [2] for single gate devices with the drain conductance substitution applied to both devices in the cascode connection. Similarly, the design philosophy employed small-signal interstage design augmented by large-signal interstage load-pull analysis and an off-chip output matching on a high dielectric constant ε_r = 37 substrate. The net result is maximized power/efficiency, a reduced chip size increasing per wafer yield and reducing per chip cost, and an overall amplifier envelope commensurate with a totally monolithic implementation.

MMIC FABRICATION

The three MMIC designs were fabricated at Harris Microwave Semiconductor using their standard MMIC process. Selective ion implantation is employed, and the N and N^+ implants used to form the MESFET structure are also used for high and low sheet resistance resistors. After formation of ohmic contacts and Schottky barrier gates, the large cross-section plated gate is formed, with this layer additionally functioning as the first level metal interconnect for transmission lines and capacitor bottom plates. Silicon Nitride dielectric used for the MIM capacitors is then deposited, followed by the second level of plated metal that forms air bridge interconnects, capacitor top plates and increased cross-section when used in conjunction with first metal for transmission lines. The substrate is thinned, via holes etched, the backside metallized, and the wafer scribed and separated into individual MMIC's.

MICROWAVE PERFORMANCE

The C/X-band variable gain amplifier (CXVGA) shown in Figure 2 consists of a six-bit SDGFET with integral bias and matching circuits. Chip size is 1.44 mm x 1.5 mm. Small signal gain is 5.5 dB $\pm$ 0.5 dB from 5.5 to 10.5 GHz with better than a 35 dB range (Figure 3). Measured input and output return losses were 6 to 12 dB from 5 to 11 GHz, with less than 3 dB maximum variation across all 64 gain/attenuation states. The precise control achieved is demonstrated in Figure 4, where the normalized amplitude performance is plotted for all 64 states from 4 to 11 GHz. Across

this band linearity error is better than 2.5%. Incidental phase variation with state is less than 6 degrees over a 20 dB control range as shown in Figure 5.

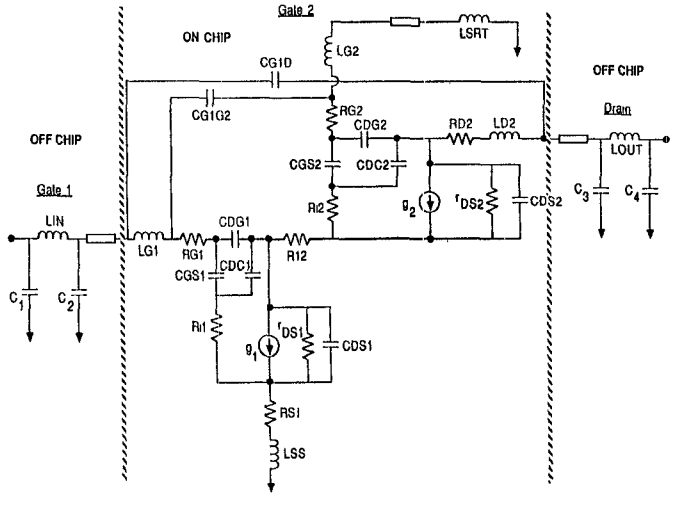
The X/K_u-band variable gain amplifier (Figure 6) shows similar performance, exhibiting a small-signal gain of 1.5 dB $\pm$ 0.5 dB over greater than an octave bandwidth from 6.4 to 15.6 Ghz as shown in Figure 7. The incidental phase shift of this circuit is less than 10 degrees from 6 to 18 GHz over a 20 dB control range. Chip size is 1.02 mm x 1.19 mm.

The X-band variable power amplifier (XVPA) shown in Figure 8 is a two-stage design consisting of a 1.4 mm segmented dual gate device of 100 µm unit finger width driving a pair of 1.4 mm devices. Gate resistors and an odd-mode stabilization resistor are employed to provide immunity to external bias connections and enhance low frequency stability (this MMIC is unconditionally stable both within and out of band). An additional resistor in the interstage dampens the Q of this network and desensitizes the interstage match to typical device variations. The gate and drain bias networks are integral to the design and are utilized as impedance matching elements. Chip size is 3.57 mm x 2.5 mm while the off-chip output matching network measures 1.7 mm x 2.1 mm. Small-signal gain is 14.5 dB $\pm$ 1.5 dB from 7.0 to 11.5 Ghz with all segments activated and is controllable over a 35 dB control range as shown in Figure 9. The circuit exhibits minimal phase variation, with less than 10 degrees incidental phase shift over a 20 dB dynamic range and less than 15 degrees over a 35 db dynamic range (Figure 10). The XVPA based upon the SDGFET approach demonstrates digitally-controlled linear transmit tapering from 0.5 watts peak with 10 to 15% power-added efficiency over the first ten dB of dynamic range, showing less degradation in efficiency than the more conventional approach, operating a saturated power amplifier in the linear region. Figure 11 depicts the output power for selected states.

REFERENCES

[1] Y.C. Hwang, D. Temme, Y.K. Chen, and R.J. Naster, "A Microwave Phase and Gain Controller with Segmented Dual Gate MESFET's in GaAs MMIC," Digest 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp 1-5, May 1984.

[2] J.J. Komiak, "Wideband C/X/K_u Power MMIC's," Digest 1987 IEEE GaAs IC Symposium, pp 215-218, October 1987.



LG1 = 26.5 pH
RG1 = 8.98 Ω
CGS1 = .1792 pF
Ri1 = 1.38 Ω
CDC1 = 38.0 fF
CDG1 = 16.9/30.8 fF
RS1 = 1.37 Ω
LSS = .035 nH
g1 = 20.882/.007 mS
τ1 = 3.08 pS
rDS1 = 505 Ω/2061 Ω
CDS1 = .0961 pF
R12 = 2.0 Ω

LG2 = 19.5 pH
RG2 = 10.48 Ω
CGS2 = .1465/.044 pF
Ri2 = 2.74 Ω
CDC2 = 40.0 fF
CDG2 = 17.4/5.6 fF
CG1D = 1.9 fF
CG1G2 = 7.2 fF
g2 = 23.939/.007 mS
τ2 = 2.03 pS
rDS2 = 72.1/88.2 Ω
CDS2 = .011 pF
RD2 = 1.35 Ω
LD2 = 21.3 pH

Figure 1: Monolithic Model of 0.5 µm x 200 µm Dual Gate MESFET Device (On/Off)

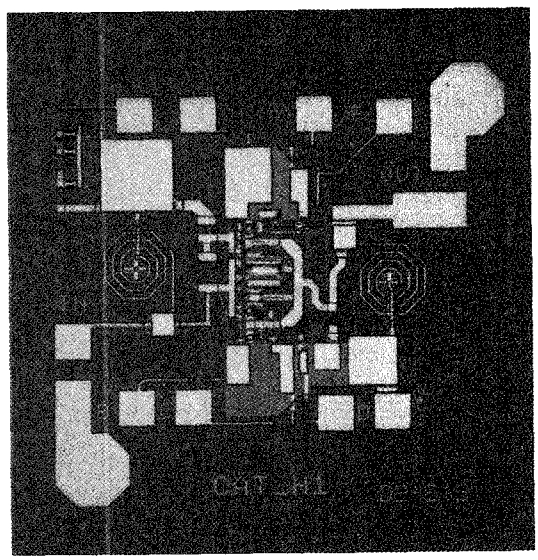


Figure 2: C/X-band Variable Gain Amplifier (CXVGA)

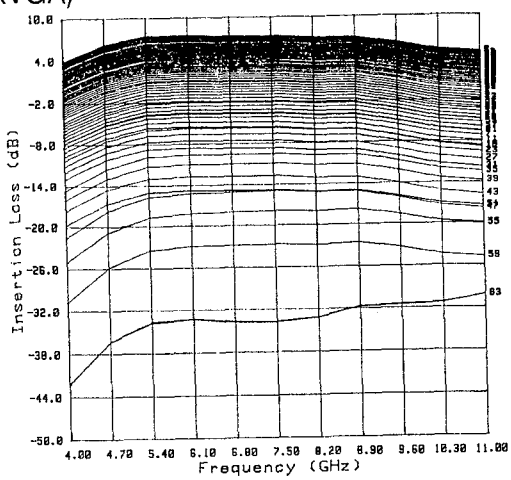


Figure 3: CXVGA Gain/Attenuation vs State

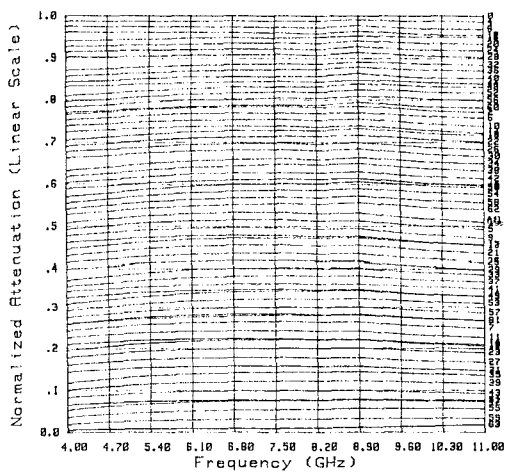


Figure 4: CXVGA Linear Scale Amplitude Across 64 States

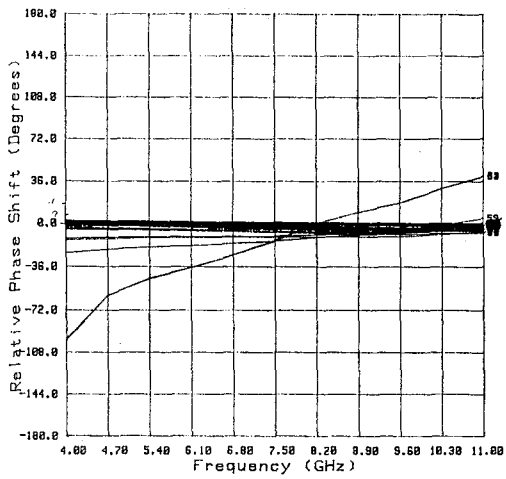


Figure 5: CXVGA Incidental Phase Shift Across 64 States

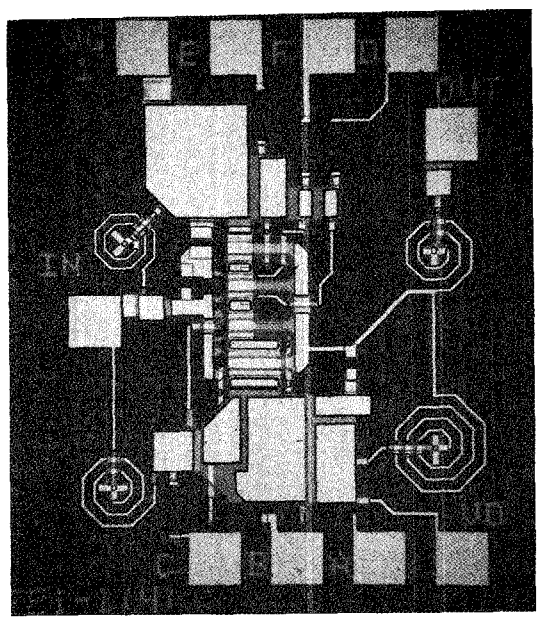


Figure 6: X/K_u-band Variable Gain Amplifier

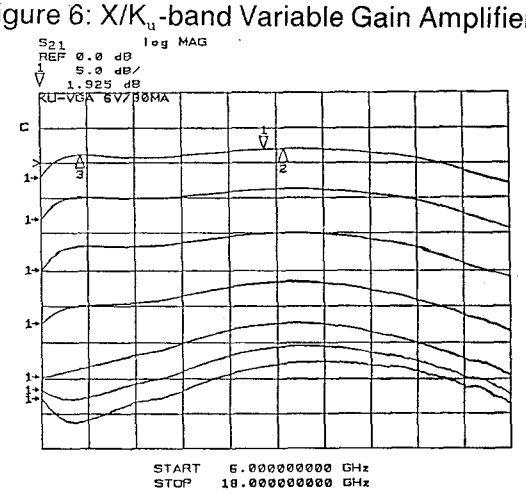


Figure 7: X/K_u-band VGA S_{21} at MSB States

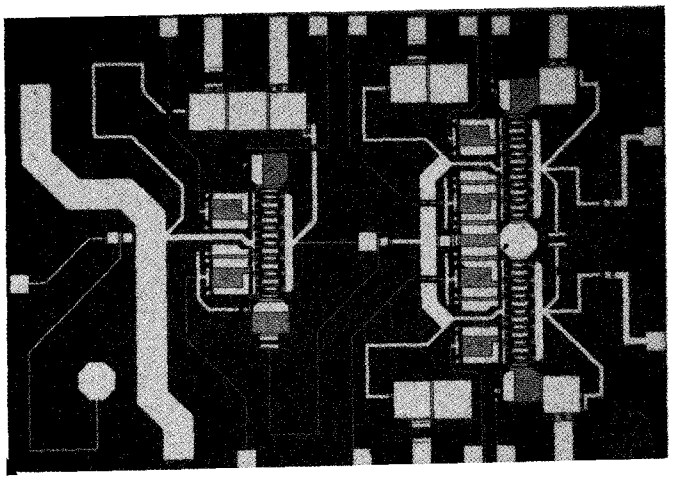


Figure 8: X-band Variable Power Amplifier (XVPA)

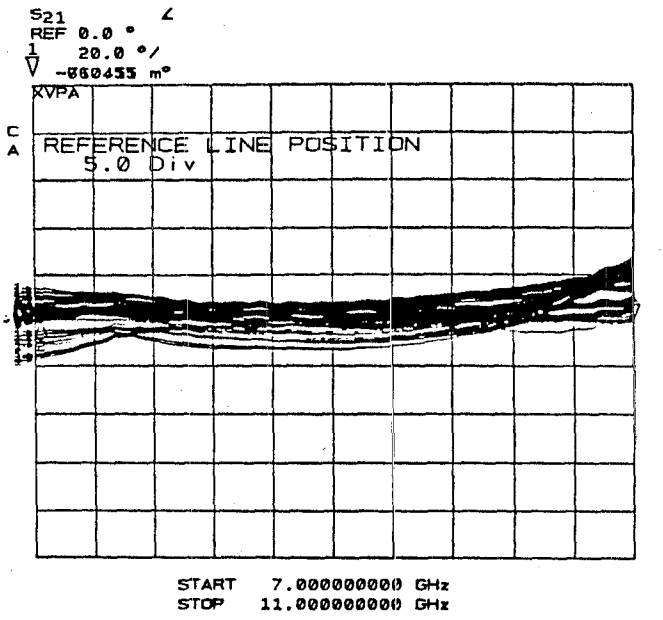


Figure 10: XVPA Incidental Phase Shift Across 64 States

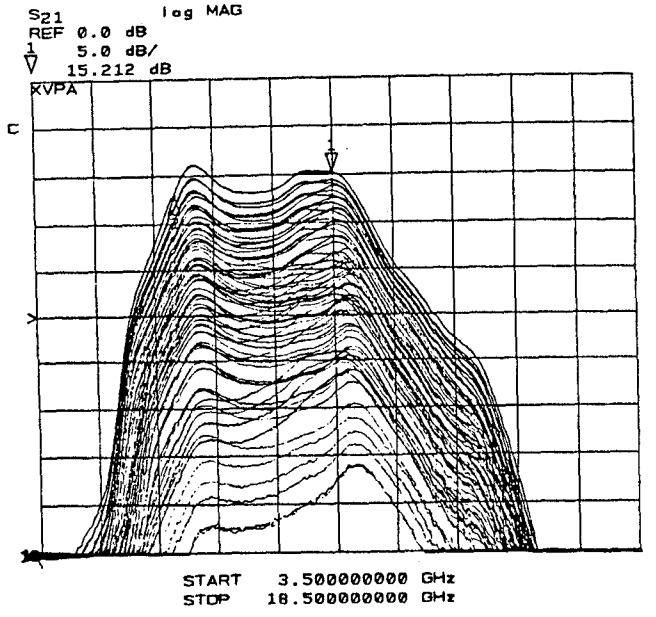


Figure 9: XVPA Gain/Attenuation Across 64 States

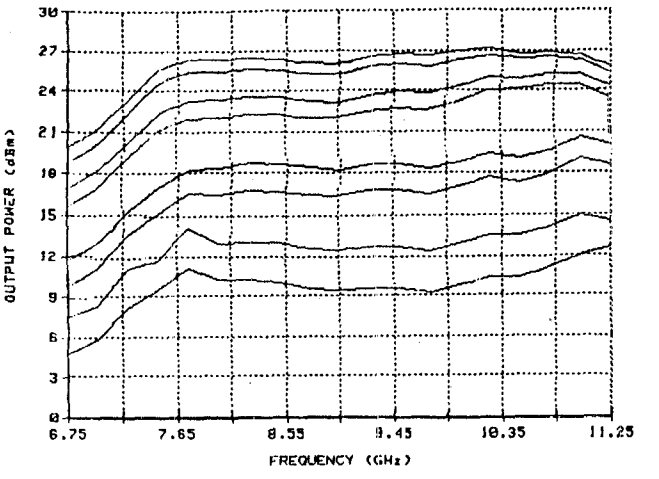


Figure 11: XVPA Output Power at Selected States